#2 Petition 3-6-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant.: Chuan Lin	)	Examiner: Not Yet Assigned
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Serial No.: Not Yet Assigned	)	Art Unit: Not Yet Assigned
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Filed: On Even Date Herewith	)	
	)	
Title: REDUCTION OF NEGATIVE BIAS TEMPERATURE INSTABILITY IN NARROW WIDTH PMOS USING F_2 IMPLANTATION	)	

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R.§ 1.97 AND 1.98

Honorable Commissioner of Patents and Trademarks
Box Patent Applications
Washington, D.C. 20231

Sir:

It is respectfully requested that the citations listed below be considered by the Patent and Trademark Office and made of official record in the above-identified application.

In the opinion of the undersigned, the below-listed citations represents the closest art known to the undersigned during the preparation of the above-identified application. This citation may be material to the examination of the subject application and is therefore submitted in compliance with the duty of disclosure defined in 37 C.F.R.§ 1.56 and 1.97.

A concise explanation of the relevance of the pertinent listed citations are set forth below.

CONCISE EXPLANATION OF THE RELEVANCE OF THE PERTINENT LISTED CITATIONS

U.S. Patent 5,909,622 is deemed pertinent for its disclosure of a method for forming a p-channel transistor, comprising:

providing a silicon substrate having a source region and a drain region spaced by a gate conductor;

exposing the drain region, the source region and the gate conductor to a nitrogen and oxygen ambient to form a nitrided oxide;

implanting a first-p-type dopant into the source region and the drain region at an angle within the range between 20^0 and 70^0 relative to upper surfaces of the source and drain regions;

depositing a source-side and a drain-side oxide upon the nitrided oxide;

removing the source-side and drain-side oxide except for spacer portions of the source-side and the drain-side oxide adjacent lateral portions of the nitrided oxide, the lateral portions being arranged adjacent opposed sidewall surfaces of the conductor; and

implanting a second p-type dopant into areas of the source region and the drain region laterally spaced from the gate conductor by the spacer portions of the source-side and drain-side oxide and the lateral portions of the nitride oxide at an angle perpendicular to upper surfaces of the source and drain regions.

A suitable p-type implant species is BF_2.

U.S. Patent 5,943,576 is deemed pertinent for its disclosure of a method of forming a portion of an MOS transistor that uses angled implant to build MOS transistors in contact holes. The method entails:

depositing a polysilicon layer over a semiconductor substrate of a first conductivity type;

depositing above the polysilicon layer a dielectric layer and a refractory metal layer;

forming a contact hole through the refractory metal layer, the dielectric layer and the polysilicon layer to expose a portion of the semiconductor substrate;

implanting a dopant at a first angle other than an angle normal to a substrate surface, to form a first source/drain region in the semiconductor substrate under the polysilicon layer on a first side of the contact hole, the first source/drain region having a conductivity type opposite the first conductivity type;

implanting the dopant at a second angle other than an angle normal to the substrate surface, to form a second source/drain region in the semiconductor substrate under the polysilicon layer on an opposite side of the first side of the contact hole, the second source/drain region having a conductivity type opposite the first conductivity type;

removing the refractory metal layer; and

forming a gate electrode in the contact hole.

The p-type dopant can be BF_2.

U.S. Patent 6,080,629, is deemed pertinent for its disclosure of ion implantation into a gate electrode layer using an implant profile displacement layer. The method of forming the gate electrode for insulated gate field effect transistor (IGFET) comprises:

providing a gate dielectric layer on an underlying semiconductor body;

forming a gate electrode layer on the gate dielectric layer;

forming a displacement layer on the gate electrode layer to form a combined displacement/gate electrode layer;

implanting a first material into the combined displacement/gate electrode layer to form an implant profile of the first material within at least the gate electrode layer; and

removing regions of the combined displacement/gate electrode layer to form a gate electrode in remaining regions.

A boron implant step may utilize BF_2.

U.S. Patent 6,117,715 is deemed pertinent for its disclosure of a method of fabricating integrated circuit field effect transistors by performing multiple implants prior to forming the gate insulating layer. The method entails:

forming a first mask pattern including first openings on a face of an integrated circuit substrate;

implanting ions into the face through the first openings to form buried implants that are remote from the face;

forming a second mask pattern in the first openings;

removing the first mask pattern from the first openings to define second openings on the face of the integrated circuit substrate;

forming surface implants in the integrated circuit substrate, adjacent the face thereof, by implanting ions into the face through the second openings; and

forming a gate insulating layer and a gate electrode in the second openings.

The p-type ions may be BF_2.

U.S. Patent 6,140,191 is deemed pertinent for its disclosure of a method of making high performance MOSFET with integrated simultaneous formation of source/drain and gate regions, comprising:

forming a first stack on the substrate and a second stack on the substrate in spaced-apart relation to the first stack, the first stack having a first layer and first and second spacers adjacent to the first layer, the second stack having a second layer and third and fourth spacers adjacent to the second layer;

forming a gate dielectric layer on the substrate between the first and second stacks;

forming a first conductor layer on the gate dielectric layer;

forming a first source/drain region beneath the first layer and a second source/drain region beneath the second layer; and

removing the first and second layers and forming a first contact on the first source/drain region and a second contact on the second source/drain region.

A p+ implant may be performed using a p-type dopant of BF_2.

U.S. Patent 6,187,643 is deemed pertinent for its disclosure of a simplified semiconductor device manufacturing process using low energy high tilt angle and high energy post-gate ion implantation. The implant parameters suitable for implementing the process includes BF_2 as the implant species.

It is known that narrow channel width devices exhibit higher NBTI/NBTS than wider channel devices for the same channel length; however, there is no known solution to this problem. For example, fluorine is known and used to suppress NBTI/NBTS by introducing it through source/drain implantation, by using a BF_2 implant. While this technique is good enough for wider channel length devices, it is not good enough for narrow channel width devices. This is in part due to the fact that, as gate oxide thicknesses get thinner, the amount of fluorine introduced through the source/drain implant is not enough for wider channel length devices - let alone narrow channel width devices. Accordingly, there is a need in the art of preparing narrow channel width devices to provide a method for reduction of negative bias temperature instability.

This Disclosure Statement under 37 C.F.R. § 1.56 and 1.97 is not construed to the effect that no other material information as defined in 37 C.F.R. § 1.56(c) exist, or that this citation constitutes prior art under U.S.C. 102 and 103.

Respectfully submitted,

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